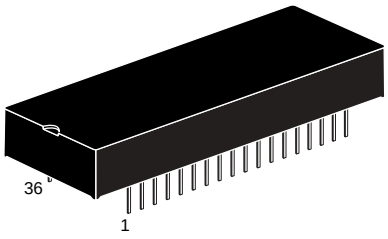
M48Z2M1Y
M48Z2M1V

5V or 3.3V, 16 Mbit (2Mb x 8) ZEROPOWER® SRAM

FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT, AND BATTERIES
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS OF DATA RETENTION IN THE ABSENCE OF POWER
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- WRITE PROTECT VOLTAGES
  (V_{PFD} = Power-fail Deselect Voltage):
  - M48Z2M1Y: V_{CC} = 4.5 to 5.5V
    $4.2V \leq V_{PFD} \leq 4.5V$
  - M48Z2M1V: V_{CC} = 3.0 to 3.6V
    $2.8V \leq V_{PFD} \leq 3.0V$
- BATTERIES ARE INTERNALLY ISOLATED UNTIL POWER IS APPLIED
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 2Mb x 8 SRAMs

Figure 1. 36-pin, DIP Module



PLDIP36 (PL)
Module

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SUMMARY DESCRIPTION

The M48Z2M1Y/V ZEROPOWER® RAM is a nonvolatile 16,777,216-bit, Static RAM organized as 2,097,152 words by 8 bits. The device combines two internal lithium batteries, CMOS SRAMs and a control circuit in a plastic 36-pin DIP, long Module.

The ZEROPOWER RAM replaces industry standard SRAMs. It provides the nonvolatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

Figure 2. Logic Diagram

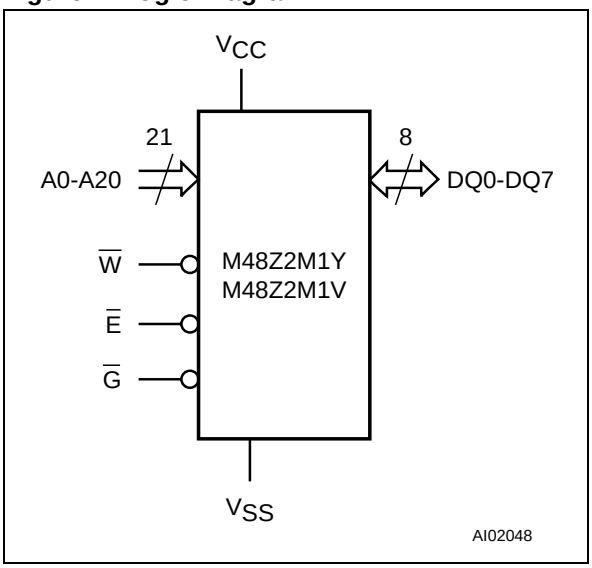


Table 1. Signal Names

A0-A20	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	WRITE Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. DIP Connections

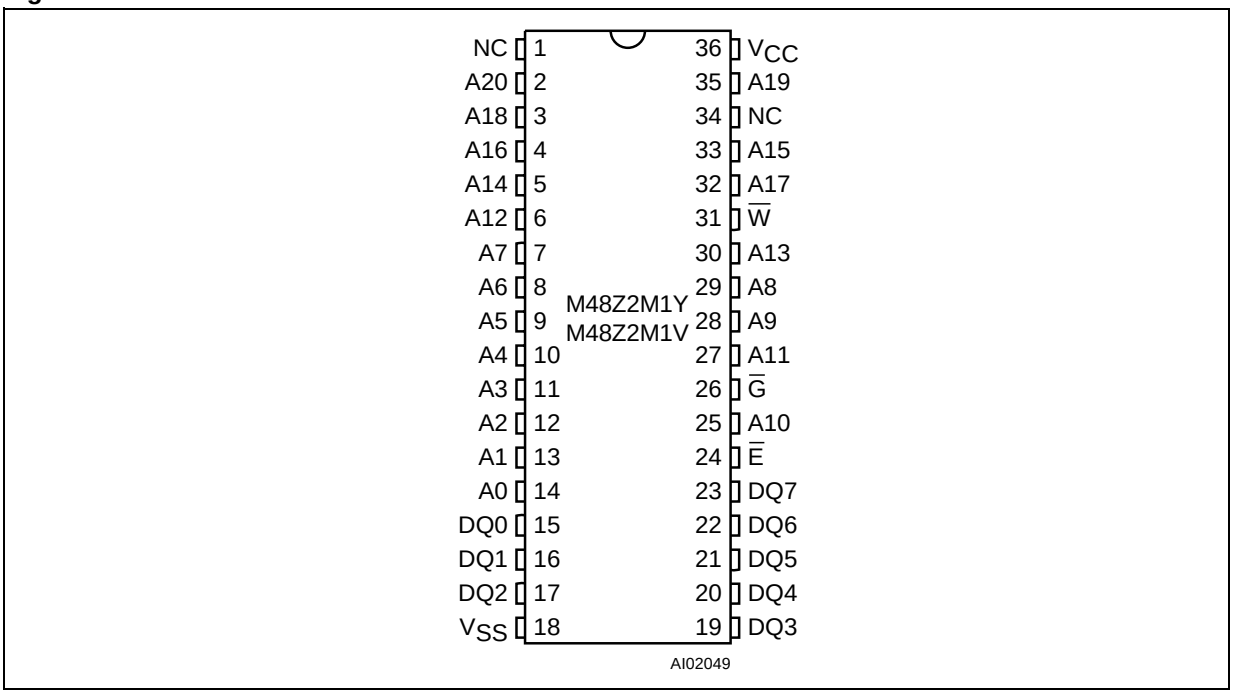
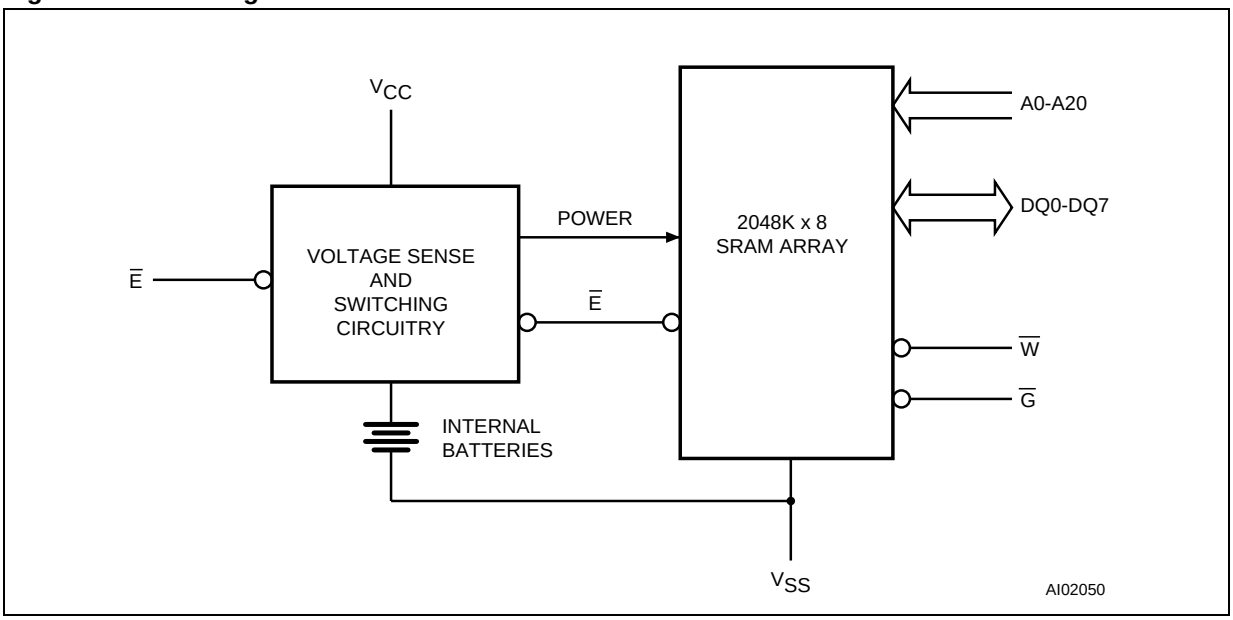


Figure 4. Block Diagram



OPERATION MODES

The M48Z2M1Y/V has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

Table 2. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	3.0 to 3.6V or 4.5 to 5.5V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery Back-up Mode

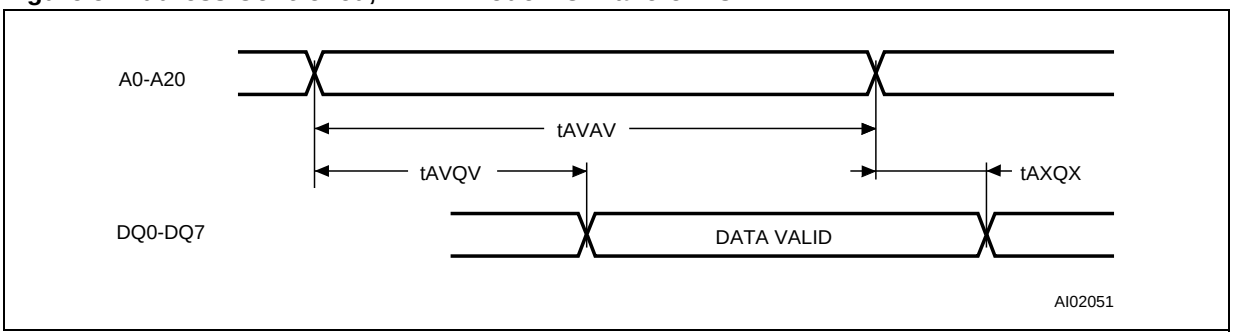
Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.

1. See Table 10., page 13 for details.

READ Mode

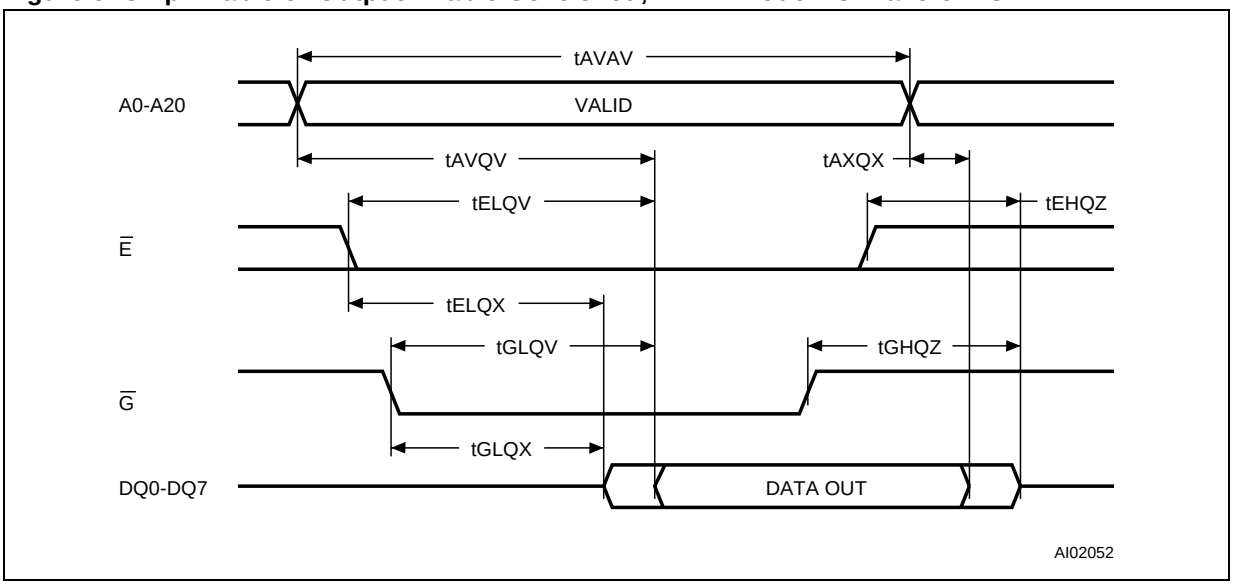
The M48Z2M1Y/V is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,777,216 locations in the static storage array. Thus, the unique address specified by the 21 Address Inputs defines which one of the 2,097,152 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ (Chip Enable) and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

Figure 5. Address Controlled, READ Mode AC Waveforms



Note: Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) = Low, WRITE Enable ($\overline{W}$) = High.

Figure 6. Chip Enable or Output Enable Controlled, READ Mode AC Waveforms



Note: WRITE Enable ($\overline{W}$) = High.

Table 3. READ Mode AC Characteristics

Symbol	Parameter[1]	M48Z2M1Y		M48Z2M1V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	READ Cycle Time	70		85		ns
t_{AVQV}[2]	Address Valid to Output Valid		70		85	ns
t_{AXQX}[2]	Address Transition to Output Transition	5		5		ns
t_{EHQZ}[3]	Chip Enable High to Output Hi-Z		30		35	ns
t_{ELQV}[2]	Chip Enable Low to Output Valid		70		85	ns
t_{ELQX}[3]	Chip Enable Low to Output Transition	5		5		ns
t_{GHQZ}[3]	Output Enable High to Output Hi-Z		25		35	ns
t_{GLQV}[2]	Output Enable Low to Output Valid		35		45	ns
t_{GLQX}[3]	Output Enable Low to Output Transition	5		5		ns

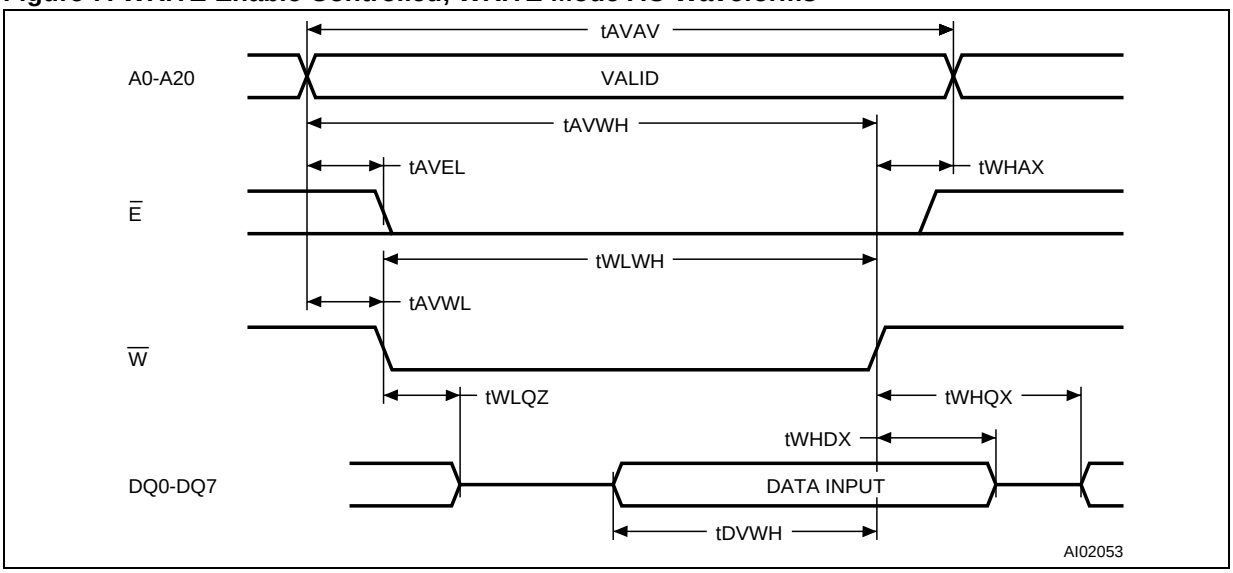
Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. C_L = 100pF or 50pF (see Figure 10., page 11).
3. C_L = 5pF (see Figure 10., page 11).

WRITE Mode

The M48Z2M1Y/V is in the WRITE Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

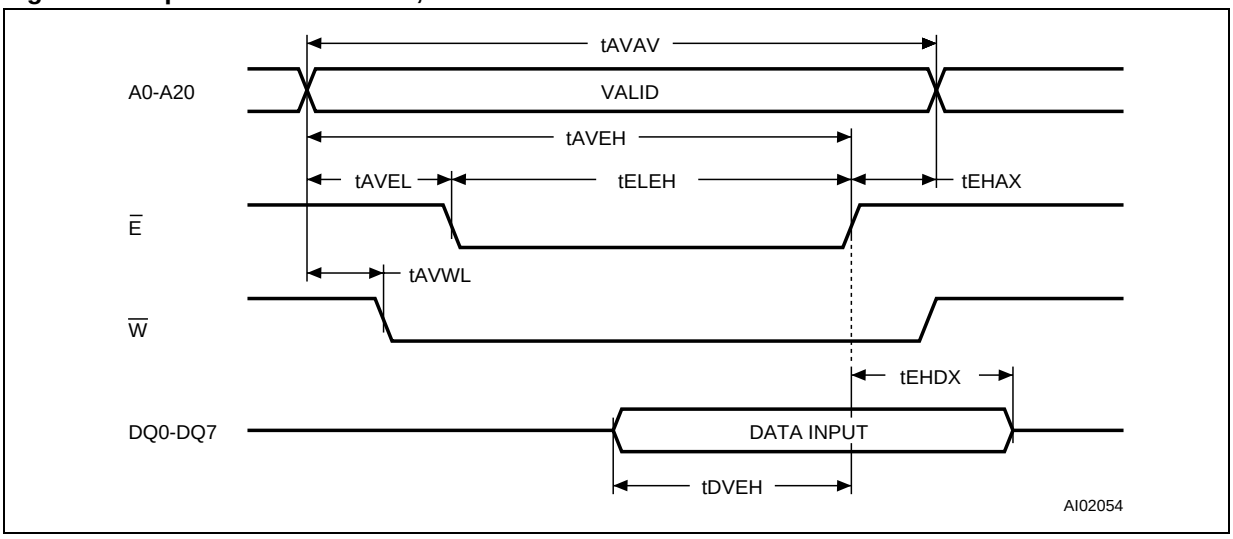
The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVEH} or t_{DVWH} prior to the end of WRITE and remain valid for t_{EHDX} or t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. WRITE Enable Controlled, WRITE Mode AC Waveforms



Note: Output Enable ($\overline{G}$) = High.

Figure 8. Chip Enable Controlled, WRITE Mode AC Waveforms



Note: Output Enable ($\overline{G}$) = High.

Table 4. WRITE Mode AC Characteristics

Symbol	Parameter[1]	M48Z2M1Y		M48Z2M1V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	WRITE Cycle Time	70		85		ns
t_{AVEH}	Address Valid to Chip Enable High	65		75		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{AVWH}	Address Valid to WRITE Enable High	65		75		ns
t_{AVWL}	Address Valid to WRITE Enable Low	0		0		ns
t_{DVEH}	Input Valid to Chip Enable High	30		35		ns
t_{DVWH}	Input Valid to WRITE Enable High	30		35		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{EHDX}	Chip Enable High to Input Transition	10		15		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		75		ns
t_{WHAX}	WRITE Enable High to Address Transition	5		5		ns
t_{WHDX}	WRITE Enable High to Input Transition	0		0		ns
t_{WHQX}[2,3]	WRITE Enable High to Output Transition	5		5		ns
t_{WLQZ}[2,3]	WRITE Enable Low to Output Hi-Z		25		30	ns
t_{WLWH}	WRITE Enable Pulse Width	55		65		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. C_L = 5pF (see Figure 10., page 11).
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Data Retention Mode

With valid V_{CC} applied, the M48Z2M1Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as “Don't care.”

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

The internal coin cells will maintain data in the M48Z2M1Y/V after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

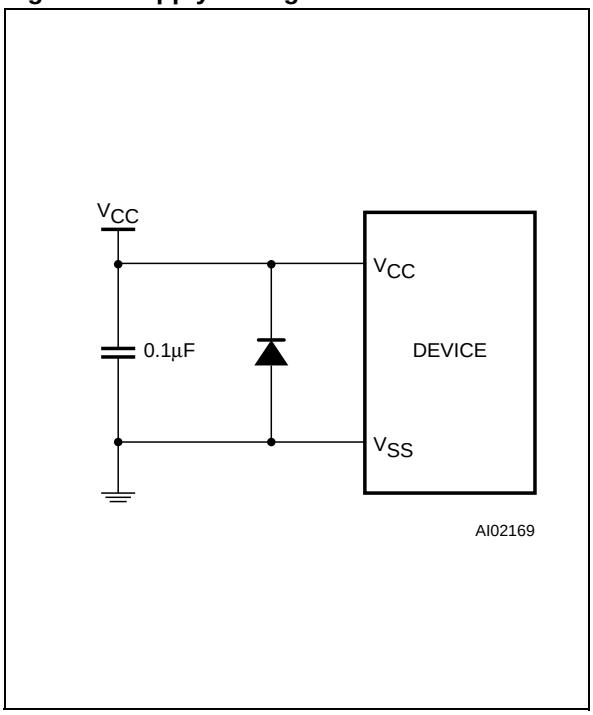
For more information on Battery Storage life refer to the Application Note AN1012.

V_{CC} Noise And Negative Going Transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in Figure 9.) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 9. Supply Voltage Protection



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)		–40 to 85	°C
T_{BIAS}	Temperature Under Bias		–40 to 85	°C
T_{SLD}(1)	Lead Solder Temperature for 10 seconds		260	°C
V_{IO}	Input or Output Voltages	M48Z2M1Y	–0.3 to 7	V
		M48Z2M1V	–0.3 to 4.6	V
V_{CC}	Supply Voltage	M48Z2M1Y	–0.3 to 7	V
		M48Z2M1V	–0.3 to 4.6	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: 1. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds). No preheat above 150°C, or direct exposure to IR reflow (or IR preheat) allowed, to avoid damaging the Lithium battery.

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC Measurement Conditions

Parameter	M48Z2M1Y	M48Z2M1V	Unit
Supply Voltage (V_{CC})	4.5 to 5.5	3.0 to 3.6	V
Ambient Operating Temperature (T_A)	0 to 70	0 to 70	°C
Load Capacitance (C_L)	100	50	pF
Input Rise and Fall Times	≤ 5	≤ 5	ns
Input Pulse Voltages	0 to 3	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 10. AC Testing Load Circuit

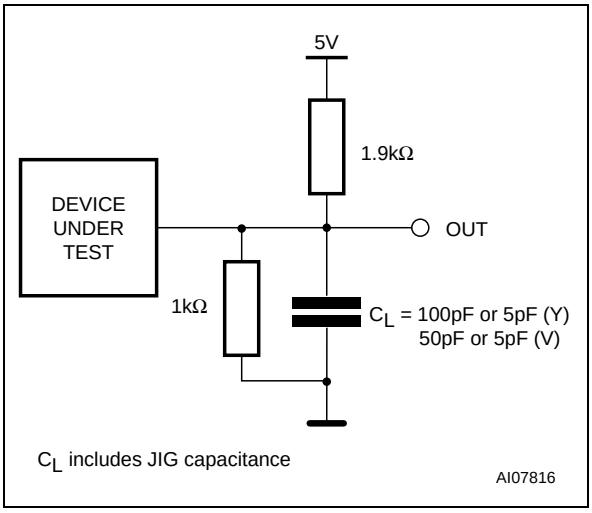


Table 7. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance		40	pF
C_{IO}[3]	Input / Output Capacitance		40	pF

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. Outputs deselected.
3. At 25°C.

Table 8. DC Characteristics

Sym	Parameter	Test Condition[1]	M48Z2M1Y		M48Z2M1V		Unit
			Min	Max	Min	Max	
I_{LI}[2]	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±4		±4	µA
I_{LO}[2]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±4		±4	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, Outputs open		140		70	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		10		2	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$		8		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	–0.3	0.6	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		2.2		V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. Outputs deselected.

Figure 11. Power Down/Up Mode AC Waveforms

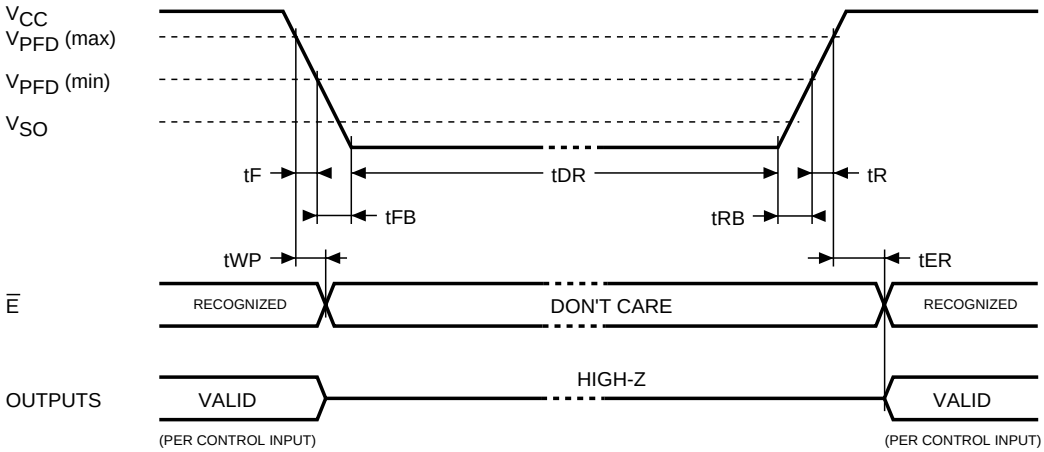


Table 9. Power Down/Up AC Characteristics

Symbol	Parameter[1]		Min	Max	Unit
t_{ER}	$\overline{E}$ Recovery Time		40	120	ms
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time		300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	M48Z2M1Y	10		µs
		M48Z2M1V	150		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time		10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	M48Z2M1Y	40	150	µs
		M48Z2M1V	40	250	µs

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than tF may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

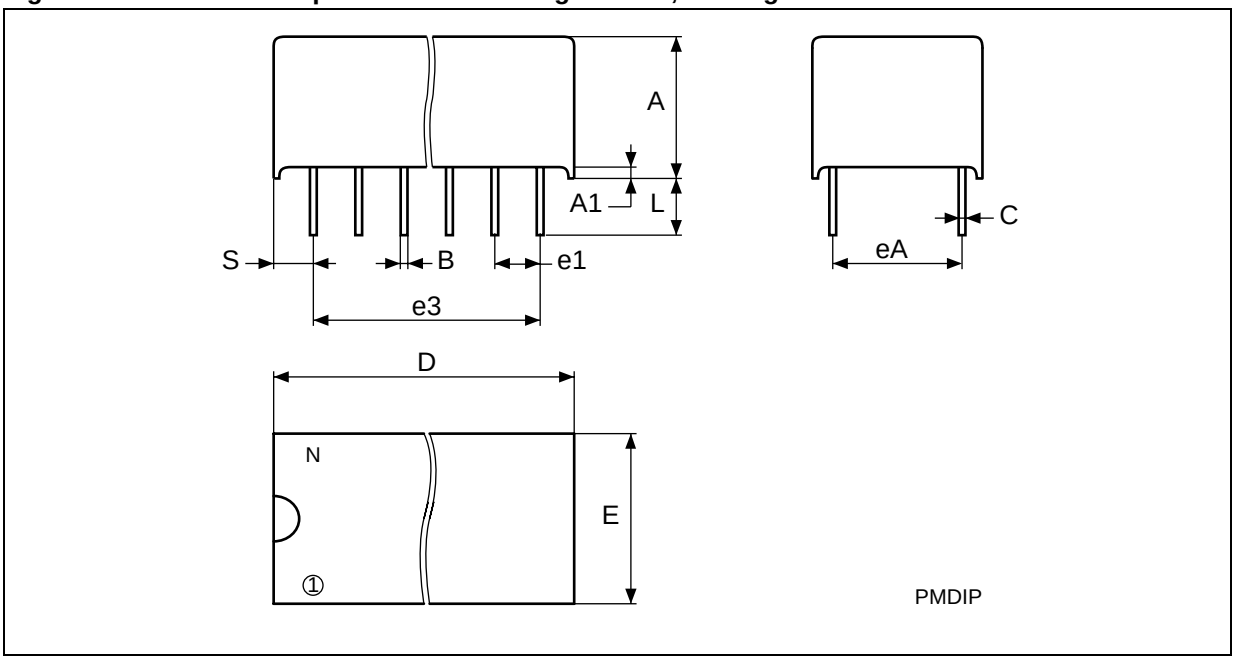
Table 10. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter[1,2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	M48Z2M1Y	4.2	4.3	4.5	V
		M48Z2M1V	2.8	2.9	3.0	V
V_{SO}	Battery Back-up Switchover Voltage	M48Z2M1Y		3.0		V
		M48Z2M1V		2.45		V
t_{DR}[3]	Expected Data Retention Time		10			YEARS

Note: 1. All voltages referenced to V_{SS}.
2. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
3. At 25°C; V_{CC} = 0V.

PACKAGE MECHANICAL INFORMATION

Figure 12. PLDIP36 – 36-pin Plastic DIP Long Module, Package Outline



Note: Drawing is not to scale.

Table 11. PLDIP36 – 36-pin Plastic DIP Long Module, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.3650	0.3748
A1		0.38			0.0150	
B		0.43	0.59		0.0169	0.0232
C		0.20	0.33		0.0079	0.0130
D		52.58	53.34		2.0701	2.1000
E		18.03	18.80		0.7098	0.7402
e1		2.30	2.81		0.0906	0.1106
e3		38.86	47.50		1.5300	1.8701
eA		14.99	16.00		0.5902	0.6299
L		3.05	3.81		0.1201	0.1500
S		4.45	5.33		0.1752	0.2098
N	36			36		

PART NUMBERING

Table 12. Ordering Information Scheme

Example: M48Z 2M1Y –70 PL 1

Device Type

M48Z

Supply Voltage and Write Protect Voltage

2M1Y = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.2 to 4.5V

2M1V = V_{CC} = 3.0 to 3.6V; V_{PFD} = 2.8 to 3.0V

Speed

–70 = 70ns (Y)

–85 = 85ns (V)

Package

PL = PLDIP36

Temperature Range

1 = 0 to 70°C

9(1) = Extended Temperature

Shipping Method

blank = Tubes

Note: 1. Contact Sales Offices for availability of Extended Temperature.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

REVISION HISTORY

Table 13. Document Revision History

Date	Rev. No.	Revision Details
July 1999	1.0	First Issue
31-Aug-00	2.0	From Preliminary Data to Data Sheet
20-Mar-02	3.0	Reformatted; Temperature information added to tables (Table 7, 8, 3, 4, 9, 10)
29-May-02	3.1	Modified “V_{CC} Noise and Negative Going Transients” text
28-Mar-03	3.2	Remove 5V/5%, add 3V part (Figure 2, 3, 10; Table 5, 6, 8, 2, 3, 4, 9, 10, 12)
02-Jul-03	3.3	Changed characteristic (Table 8)
18-Feb-05	4.0	Reformatted; IR reflow update (Table 5)